Amendments to the Specification

Please amend paragraph [0045] of the specification as follows:

Marking host processor 402, in a preferred embodiment, is a personal computer. In alternate embodiments, marking host processor 402 could be an inventory management system, a retail system such as a point of sale (POS) terminal, a cash register, or any processing device. Marking host processor 402 enables users to interface with marking node 302.~~402.~~ Marking host processor also stores information regarding marking activity, articles, and security data.

Please amend paragraph [0052] of the specification as follows:

In a preferred embodiment, verification control processor 504 is a PCMCIA peripheral card that connects to verification host processor 502. Verification control processor 504 performs processing tasks necessary to verify the authenticity of articles. These processing tasks include encryption, image processing, communication with verification host processor 502, and the control of other verification node 304 components such as reader 506.~~ and printer 508.~~

Please amend paragraph [0054] of the specification as follows:

In a preferred embodiment, reader 506 reads latent markings 104~~304~~ from first counterfeit resistant articles 100. Therefore, reader 506 is capable of reading infrared patterns. Reader 506 includes one or more optical scanners that are implemented with charge-coupled devices (CCDs). In alternate embodiments, reader 506 is capable of reading other markings such as bar codes, magnetic strips and text.

Please amend paragraph [0055] of the specification as follows:

FIG. 6 illustrates components of a security management node 306 according to a preferred embodiment. Security management node ~~106~~ 306 includes a key manager 602, a transaction manager 604, an access manager 606, and an article database 608. These components can be implemented with hardware, software, firmware, or any combination thereof.

Please amend paragraph [0068] of the specification as follows:

FIG. 9 illustrates a counterfeit detection process according to an embodiment of the present invention. In a preferred embodiment, this process is performed by verification node 304~~104~~ and begins with step 904. This process will be described with respect to both first counterfeit resistant article 100 and second counterfeit resistant article 200.